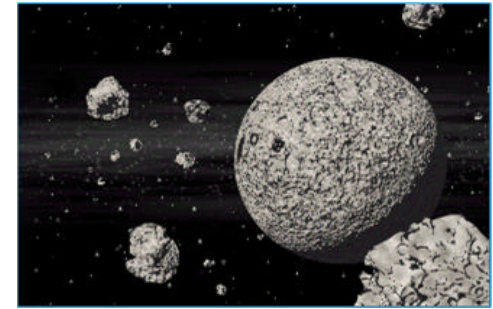


# Asteroid-Z

## MS-7423N1

Version 0C



### CPU:

Wolfdale, Conroe, Conroe-1M,  
; TDP max=65W, FSB 1333/1066/800

### System Chipset:

Intel Q45 (North Bridge)  
Intel ICH10DO (South Bridge)

### On Board Chipset:

BIOS -- SPI FLASH 32MB  
HD AUDIO Codec -- ALC262  
LPC Super I/O -- SMSC SCH5617  
LAN --INTEL 82567LM Boazman  
Clock GEN-IDTCV184-2  
TPM - SLB9635 TT1.2  
PCMCIA - Ricon 5C812/PCI

### Expansion Slots:

Half mini PCIE SLOT \* 1

### Main Memory:

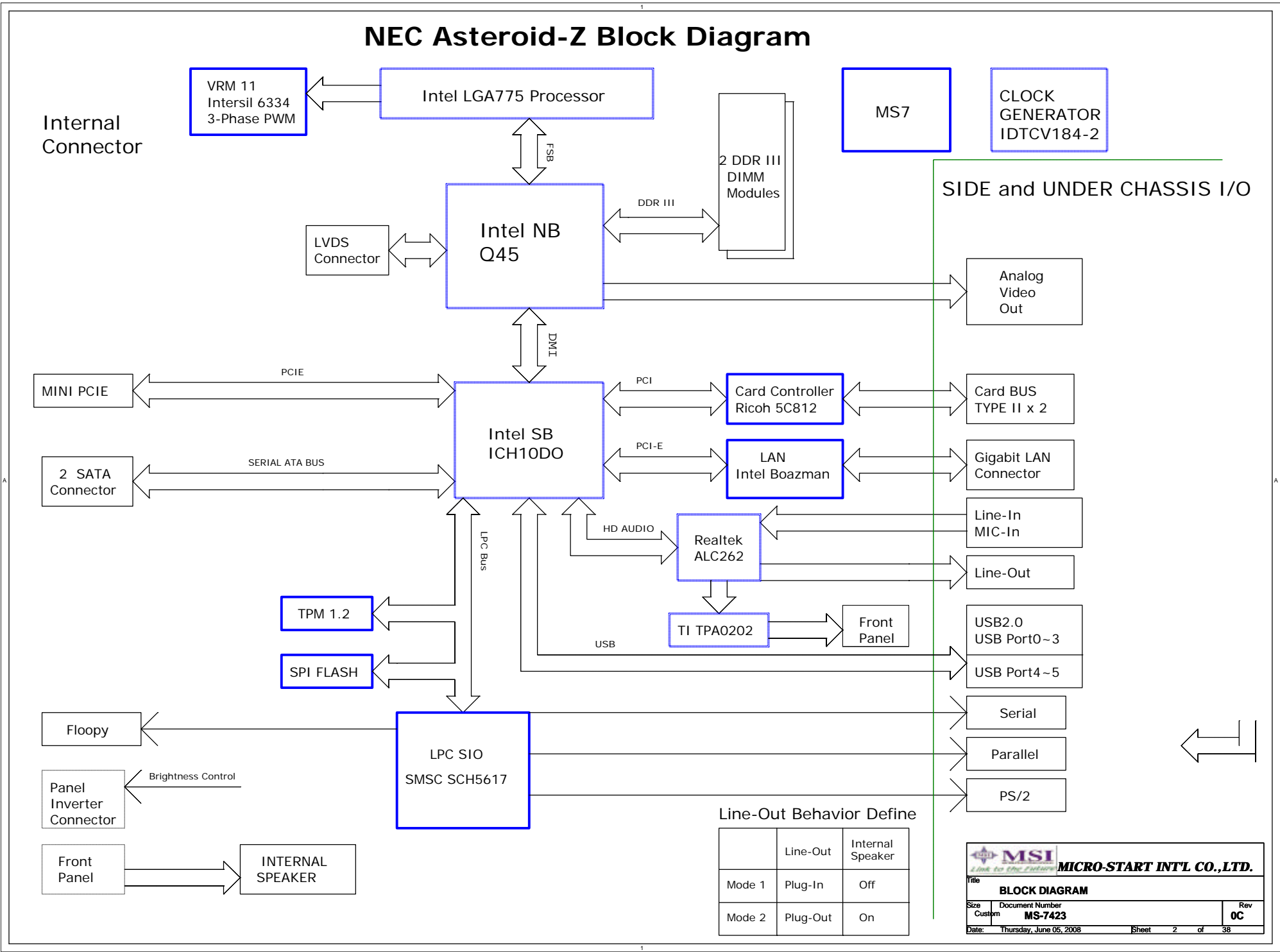
DDR III \* 2 - 1066 w/o ECC

### Intersil PWM:

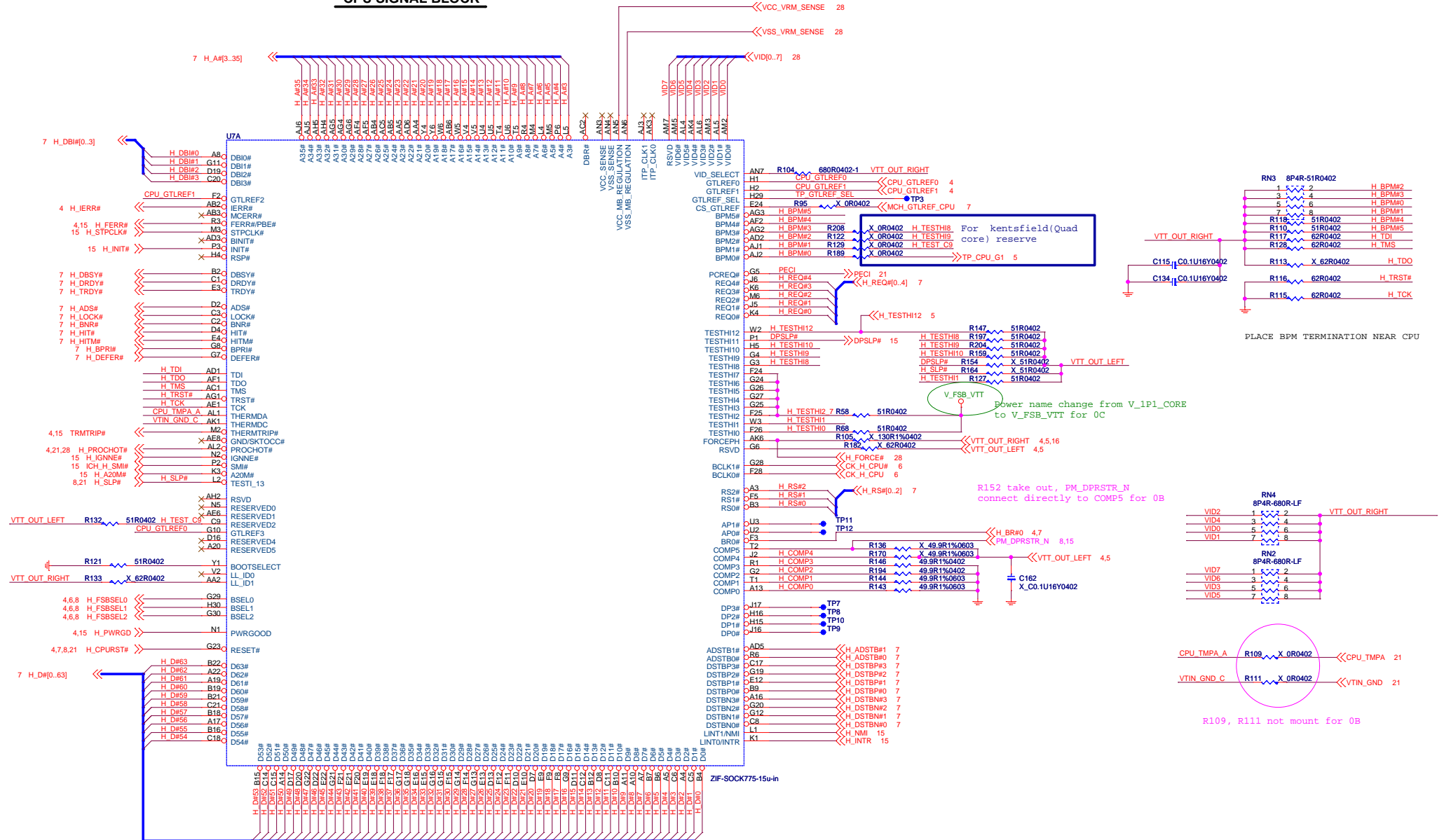
Controller: Intersil 6334 3Phase

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BLOCK DIAGRAM	2
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NEC Asteroid-Z Block Diagram

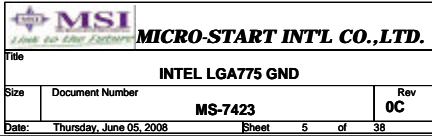


### CPU SIGNAL BLOCK



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)

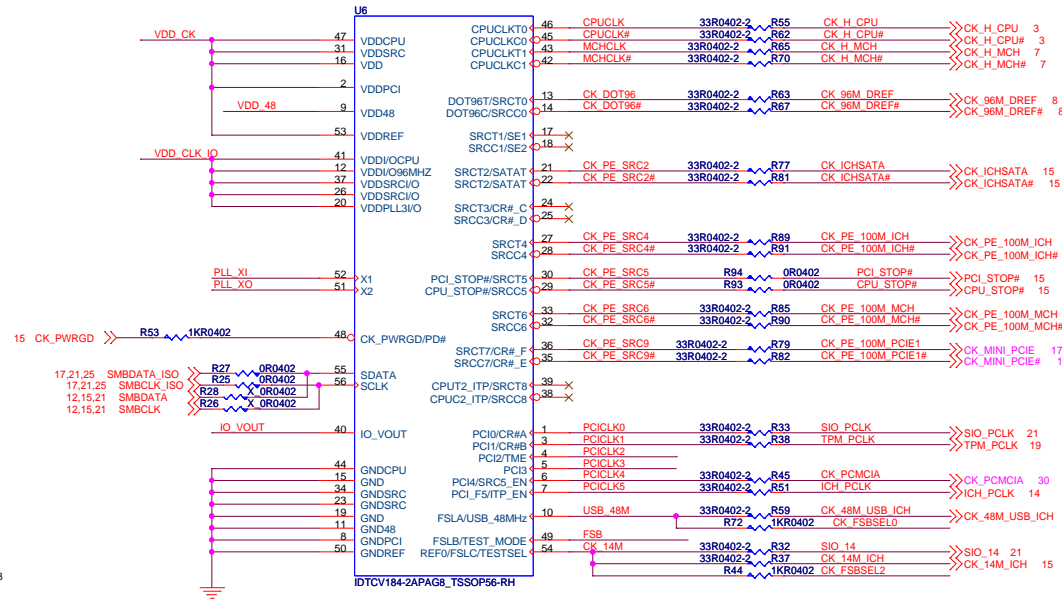




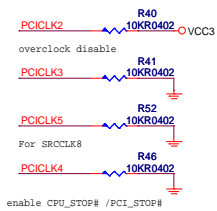
## ~~CLOCK Generator -~~ IDTCV184-2

### VDD\_CK Decoupling

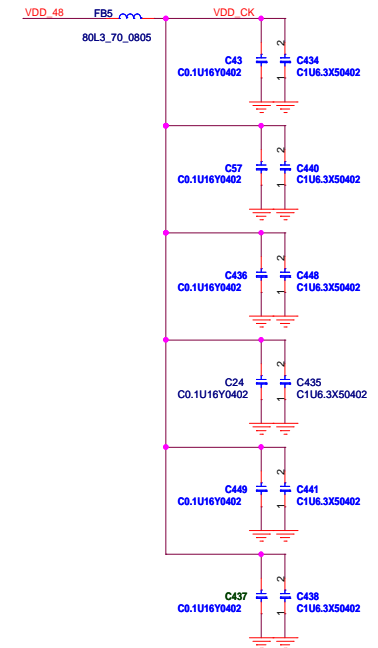
Place near each VDD\_CK Pins



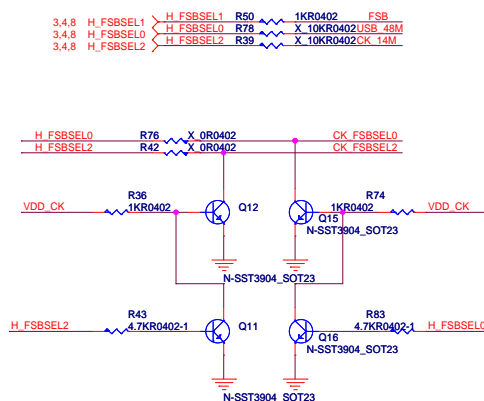
### Strapping resistor



C28, C29 are changed from 27pF to 47pF for 0B

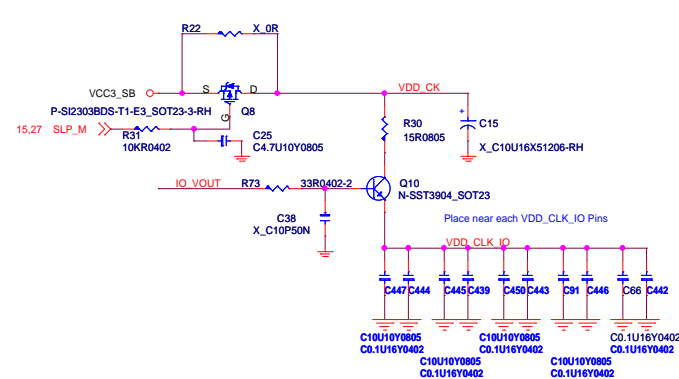


### CPU Frequency select

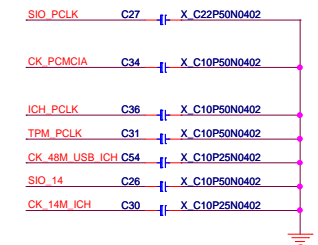


FS <sub>0</sub> C <sup>1</sup> B0b7	FS <sub>0</sub> B <sup>1</sup> B0b6	FS <sub>0</sub> A <sup>2</sup> B0b5	CPU MHz
0	0	0	266.66
0	0	1	123.33
0	1	0	200.00
0	1	1	166.66
1	0	0	323.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Fast review

### VDD\_CK & VDD\_CLK\_IO Power



For EMI  
reserver



**MICRO-START INT'L CO.,LTD.**

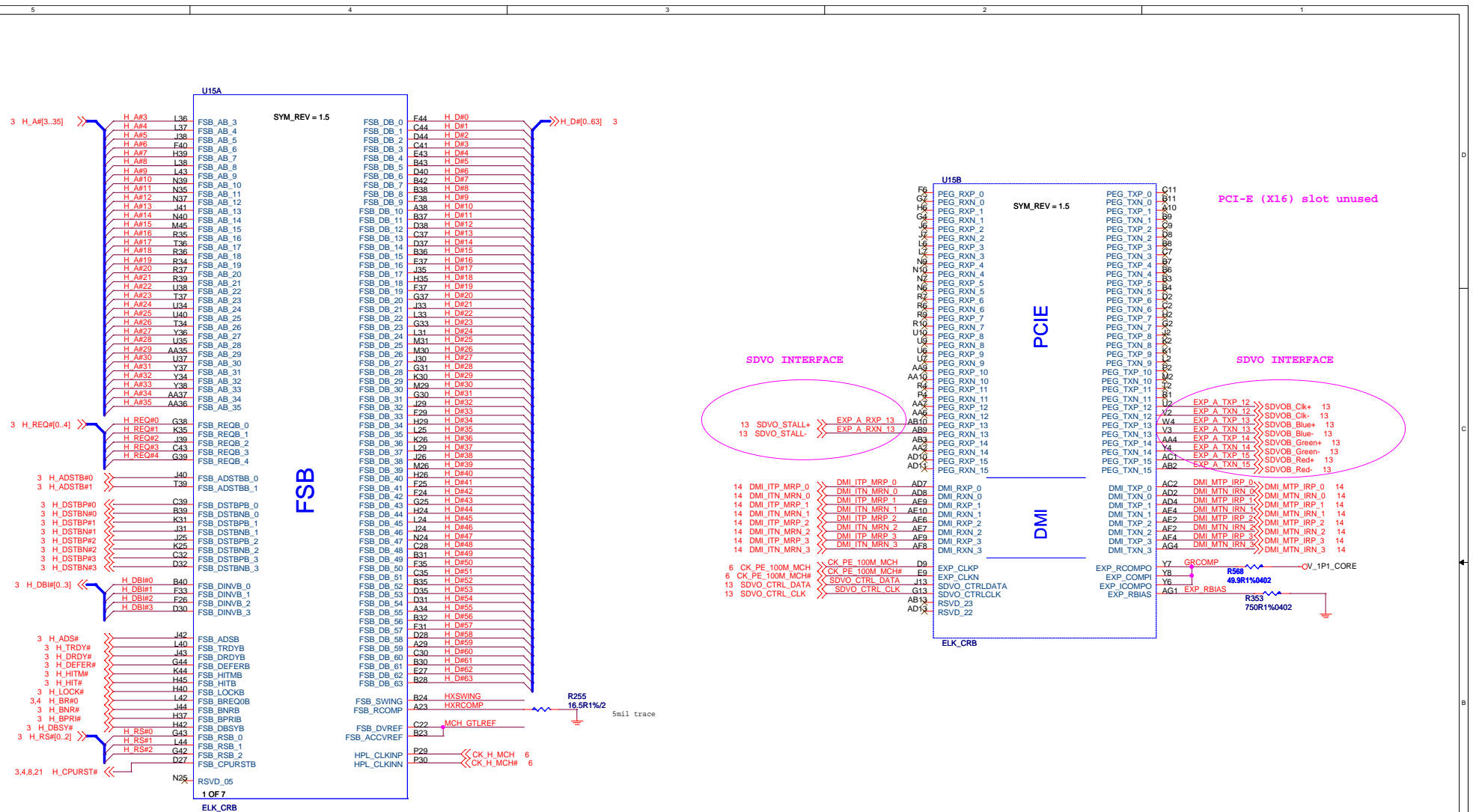
Title \_\_\_\_\_

**CLOCK Generator-IDTCV184-2APAG8**

MS-7423

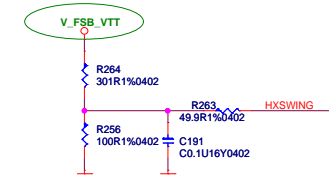
Rev	
0C	

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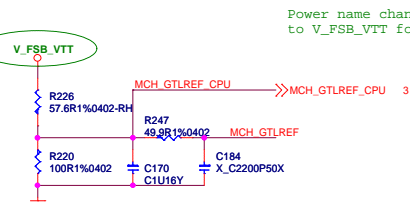


HD\_SWING VOLTAGE \*10 MIL TRACE , 7 MIL SPACE\* HD\_SWING S/B 1/4\*VTT +/- 2%

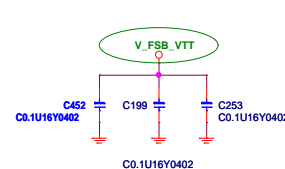
PLACE DIVIDER RESISTOR NEAR VTT



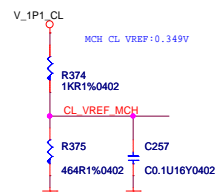
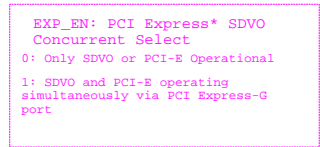
GTREF VOLTAGE SHOULD BE 0.63\*VTT=0.8V 100 OHM OVER 200 RESISTORS



Power name change from V\_lPl\_CORE to V\_FSB\_VTT for 0C







```
ITPM_ENB
Integrated TPM Enable:
0=Enable iTPM
1=Disable iTPM
```

DualX8\_Enable  
0=2X8 PCIe Ports Enable  
1=1X16 PCIe Port Enable

```

DEMO BOARD CHANGE
Primary_PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot

```

PIN	H	L	Description
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TCFN	Enable	Disable	T.S. confidentiality

The image displays three circuit diagrams illustrating decoupling capacitor connections for different power planes:

- VCC\_DDR:** This diagram shows a power plane with four decoupling capacitors connected in parallel to ground. The capacitors are labeled C322, C317, C321, and C320, all with a value of 1U1010X.
- VTT\_DDR:** This diagram shows a power plane with two decoupling capacitors connected in parallel to ground. The capacitors are labeled C318 (C4.7U10Y0805) and C339 (X\_C4.7U10Y0805).
- V\_3P3\_CL:** This diagram shows a power plane with two decoupling capacitors connected in parallel to ground. The capacitors are labeled C341 (C0.1U16Y0402) and C350 (C0.1U16Y0402).

The image displays three circuit diagrams illustrating the placement of decoupling capacitors for different power planes:

- VCC\_DDR:** Shows a power plane with four decoupling capacitors (C347, C1U10X, C344, C1U10X, C343, C1U10X, C340, C1U10X) connected to ground.
- VTT\_DDR:** Shows a power plane with two decoupling capacitors (C319, C4.7U10Y0805, C342, X\_C4.7U10Y0805) connected to ground.
- V\_3P3\_CL:** Shows a power plane with two decoupling capacitors (C351, C0.1U16Y0402, C335, C0.1U16Y0402) connected to ground.

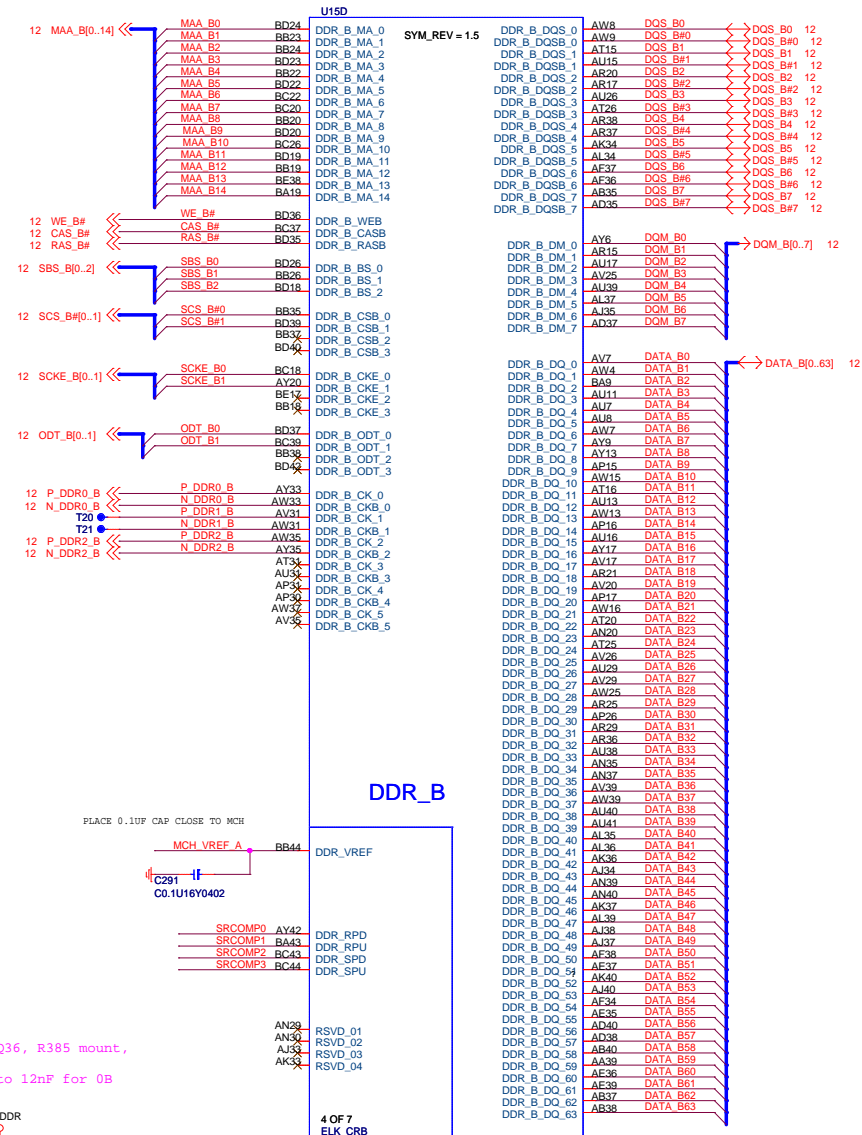
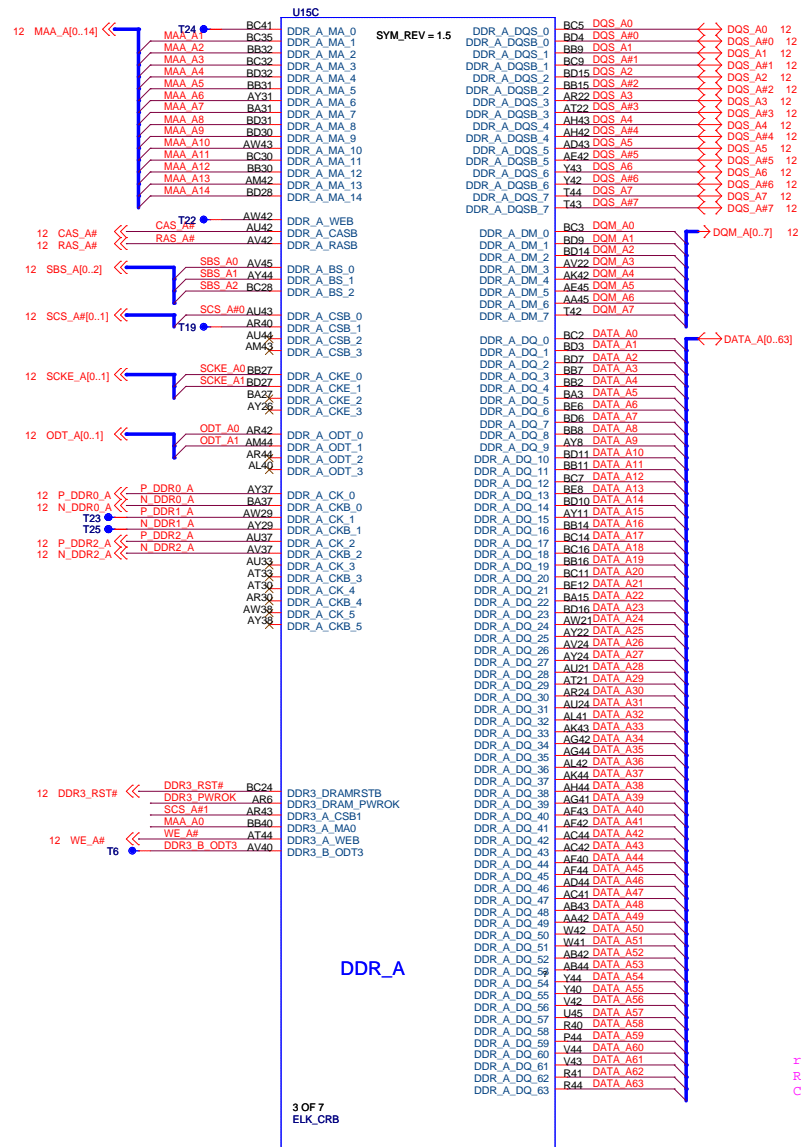
EC60 change from 1000uF to 820uF for 0B

[illegible]

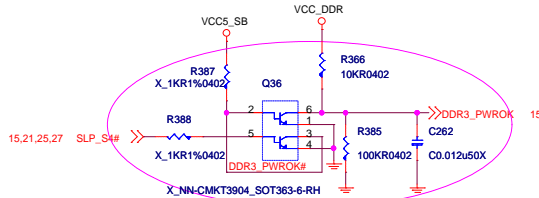
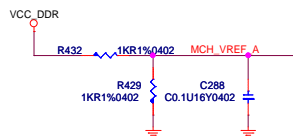
PDG:page 438 ,Please put near PWM

R158 no mount, Q27 mount, remove R142, add Q34 for 0B

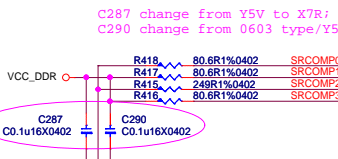
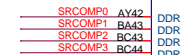
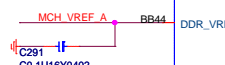




remove Q54, Q56, add Q36, R385 mount,  
R387& R388 not mount  
C262 change from 1uF to 12nF for 0B



PLACE 0.1uF CAP CLOSE TO MCH



DDR\_B

DDR\_VREF

DDR\_RPD

DDR\_RPU

DDR\_SPD

DDR\_SPU

AN39

AN30

AN33

AN34

AN35

AN36

AN37

AN38

AN39

AN40

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AN42

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AN45

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AN248

AN249

# POWER

Power name change from  
V\_1P1\_CORE to  
V\_FSB\_VTT for 0C

V\_FSB\_VTT

V\_1P1\_CORE

U15F

VTT\_FSB\_01  
VTT\_FSB\_02  
VTT\_FSB\_03  
VTT\_FSB\_04  
VTT\_FSB\_05  
VTT\_FSB\_06  
VTT\_FSB\_07  
VTT\_FSB\_08  
VTT\_FSB\_09  
VTT\_FSB\_10  
VTT\_FSB\_11  
VTT\_FSB\_12  
VTT\_FSB\_13  
VTT\_FSB\_14  
VTT\_FSB\_15  
VTT\_FSB\_16  
VTT\_FSB\_17  
VTT\_FSB\_18  
VTT\_FSB\_19  
VTT\_FSB\_20  
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VTT\_FSB\_27  
VTT\_FSB\_28  
VTT\_FSB\_29  
VTT\_FSB\_30  
VTT\_FSB\_31  
VTT\_FSB\_32  
VTT\_FSB\_34  
VTT\_FSB\_35  
VTT\_FSB\_36

V\_1P5\_ICH R235 VCCD CRT B20 VCCDQ\_CRT

VCCA\_GPLL B16 VCCAPLL\_EXP  
VCCA\_MPLL A21 VCCA\_MPLL  
VCCA\_HPLL B22 VCCA\_HPLL  
VCCA\_GPLL D12 VCCDPLL\_EXP  
V\_1P1\_HPL U33 VCCD\_HPLL  
VCCA\_DPLLA D20 VCCA\_DPLLA  
VCCA\_DPLLB C20 VCCA\_DPLLB

V\_3P3\_DAC\_FILTERED D19 VCCA\_DAC\_01  
B19 VCCA\_DAC\_02

V\_1P5\_EXP\_FB VCC3\_3.1 E19 VCC\_EXP  
A17

remove R365 for 0C

V\_1P5\_ICH R381 VCCA\_VRM\_EXP AG2

V\_1P5\_ICH AR2 VCC\_HDA B17 VSS\_369

V\_CKDDR AK32 VCC\_SMCLK\_04  
AL31 VCC\_SMCLK\_03  
AL32 VCC\_SMCLK\_02  
AM31 VCC\_SMCLK\_01  
AM30 VCCSM\_LDDR

C251 C1U16Y

V\_1P1\_CL R362 V\_1P1\_CL OR0603

V\_1P1\_CL  
Separate when AMT is supported

If has noise stuff L01-1006014-J07  
,IND INDUCTOR,10uH,104,0805,100mA,1.0ohm,ROHS COMPLIANCE

remove R257;  
L7 change from 10uH to 0ohm for 0B

V\_1P1\_CORE L7 V\_1P1\_CL  
C194 C10U10Y0805  
C195 C0.1U16Y0402

If has noise stuff L01-22A7013-M09  
,IND INDUCTOR,2.2uH,204,0603,120mA,0.4ohm,ROHS COMPLIANCE

V\_1P1\_CL R209 V\_1P1\_CL  
OR0603 VCCA\_MPLL  
R210 V\_1P1\_CL  
R212 VCCA\_MPLL

C147 C10U10Y0805

If has noise stuff L01-27BA013-M09  
,IND INDUCTOR,0.27uH,54,0603,110mA,3.4ohm,ROHS COMPLIANCE

V\_1P1\_CL R211 V\_1P1\_CL  
OR0603 VCCA\_HPLL  
C161 C22U6.3Y

VCC\_SM\_01  
VCC\_SM\_02  
VCC\_SM\_03  
VCC\_SM\_04  
VCC\_SM\_05  
VCC\_SM\_06  
VCC\_SM\_07  
VCC\_SM\_08  
VCC\_SM\_09  
VCC\_SM\_10  
VCC\_SM\_11  
VCC\_SM\_12  
VCC\_SM\_13  
VCC\_SM\_14  
VCC\_SM\_15

V\_1P1\_CORE  
VCC\_98  
VCC\_99  
VCC\_100  
VCC\_101  
VCC\_102  
VCC\_103  
VCC\_104

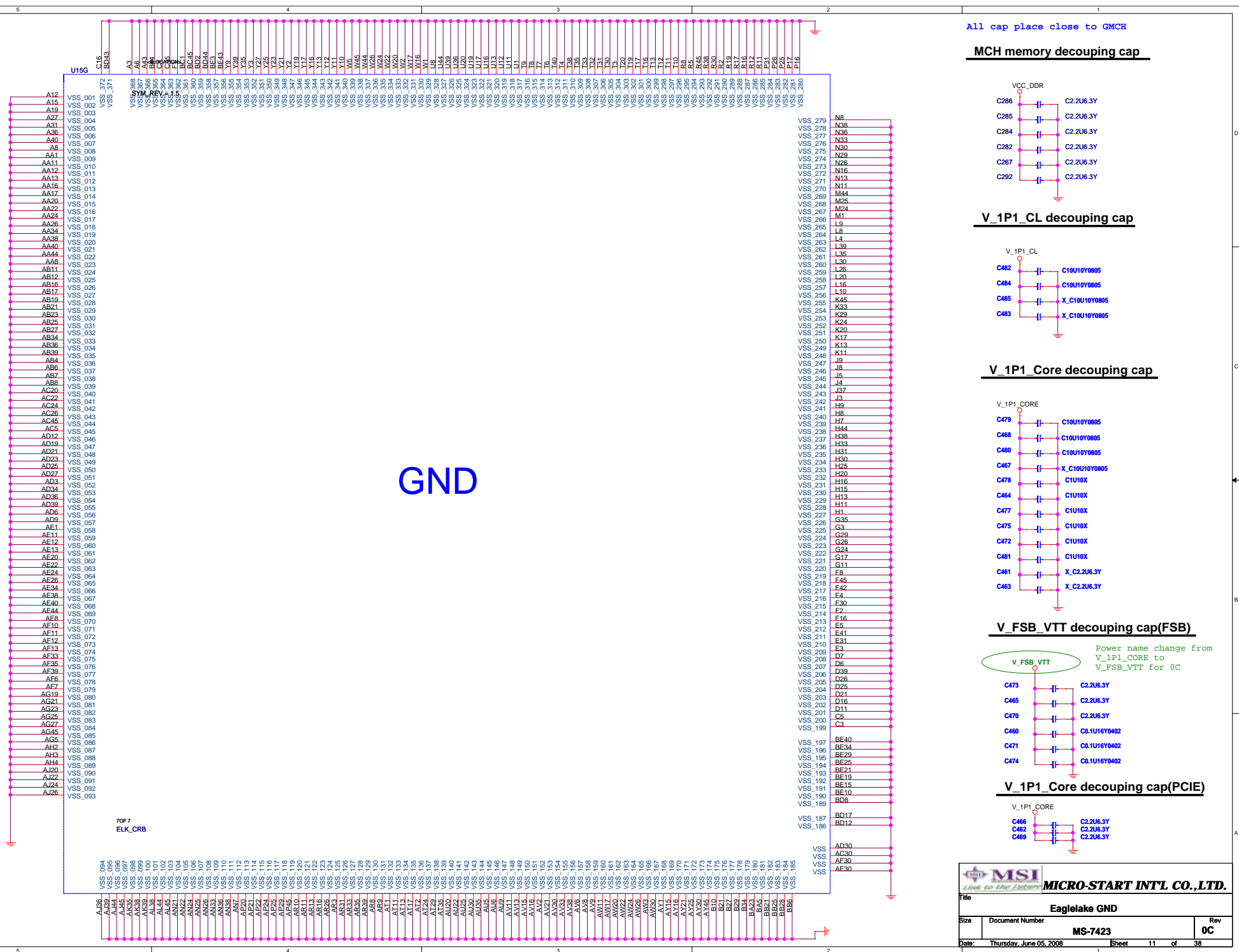
VCC\_EXP\_1  
VCC\_EXP\_2  
VCC\_EXP\_3  
VCC\_EXP\_4  
VCC\_EXP\_5  
VCC\_EXP\_6  
VCC\_EXP\_7  
VCC\_EXP\_8  
VCC\_EXP\_9  
VCC\_EXP\_10  
VCC\_EXP\_11  
VCC\_EXP\_12  
VCC\_EXP\_13  
VCC\_EXP\_14  
VCC\_EXP\_15  
VCC\_EXP\_16  
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VCC\_EXP\_24  
VCC\_EXP\_25  
VCC\_EXP\_26  
VCC\_EXP\_27  
VCC\_EXP\_28  
VCC\_EXP\_29  
VCC\_EXP\_30  
VCC\_EXP\_31  
VCC\_EXP\_32  
VCC\_EXP\_33  
VCC\_EXP\_34  
VCC\_EXP\_35  
VCC\_EXP\_36  
VCC\_EXP\_37  
VCC\_EXP\_38

VCC\_DDR

VCC\_SM\_01  
VCC\_SM\_02  
VCC\_SM\_03  
VCC\_SM\_04  
VCC\_SM\_05  
VCC\_SM\_06  
VCC\_SM\_07  
VCC\_SM\_08  
VCC\_SM\_09  
VCC\_SM\_10  
VCC\_SM\_11  
VCC\_SM\_12  
VCC\_SM\_13  
VCC\_SM\_14  
VCC\_SM\_15

V\_1P1\_CORE

V\_1P1\_CORE



All cap place close to GMCH

### MCH memory decoupling cap

### V\_1P1\_CL decoupling cap

### V\_1P1\_Core decoupling cap

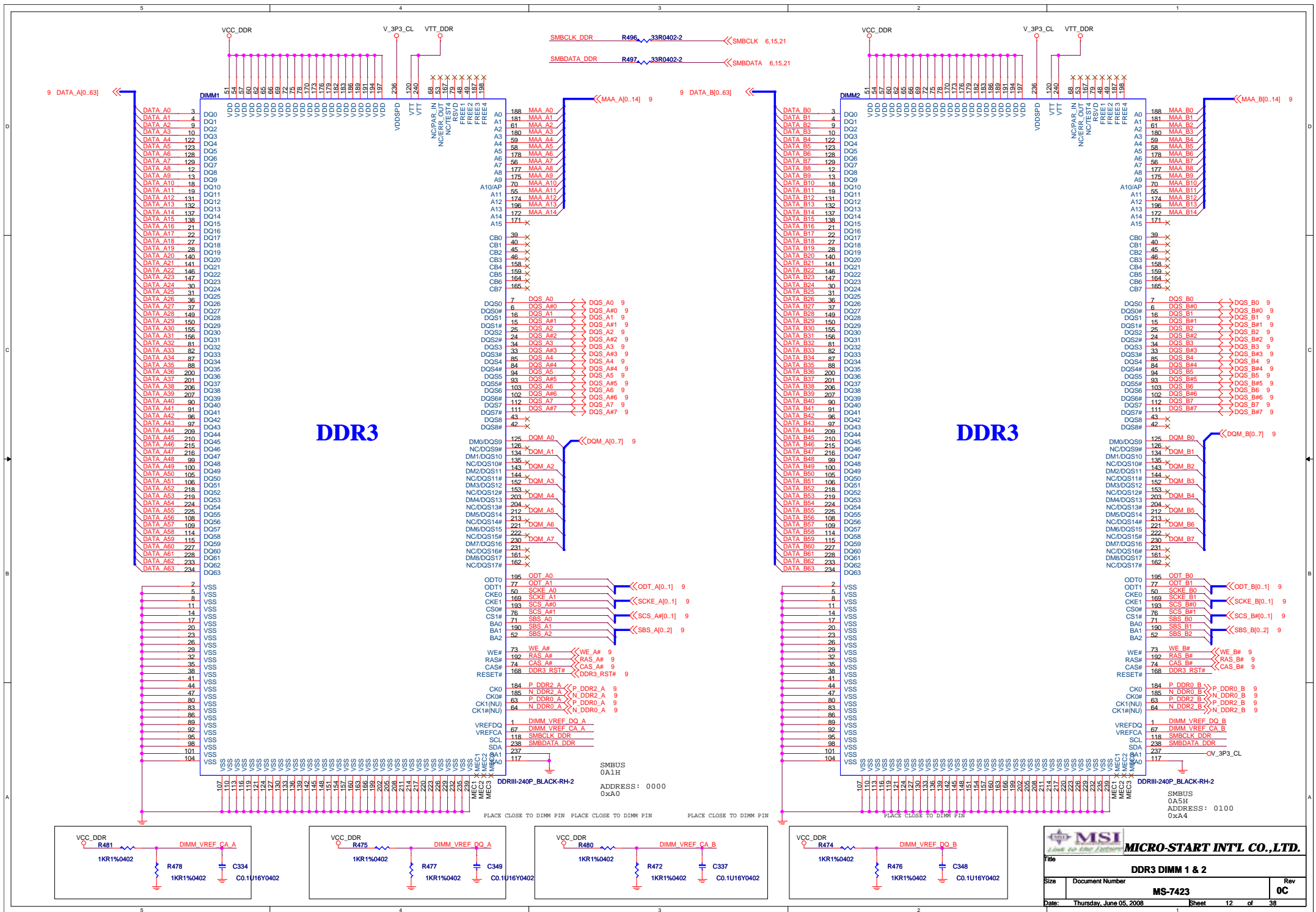
### V\_FSB\_VTT decoupling cap(FSB)

### V\_1P1\_Core decoupling cap(PCIE)

Power name change from V\_1P1\_CORE to V\_FSB\_VTT for 0C

**MICRO-START INT'L CO.,LTD.**

Title		
Eaglelake GND		
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	MS-7423	0C
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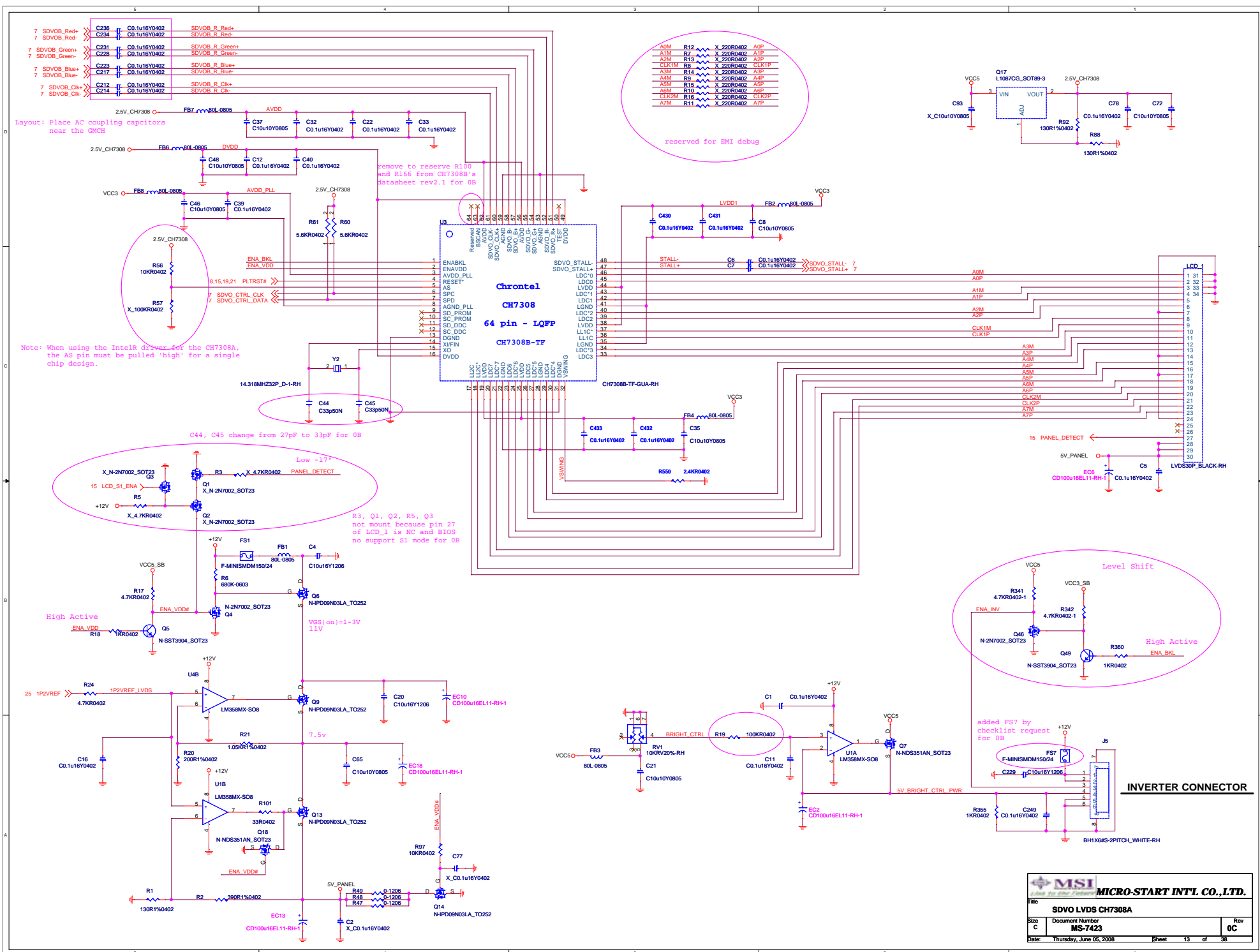
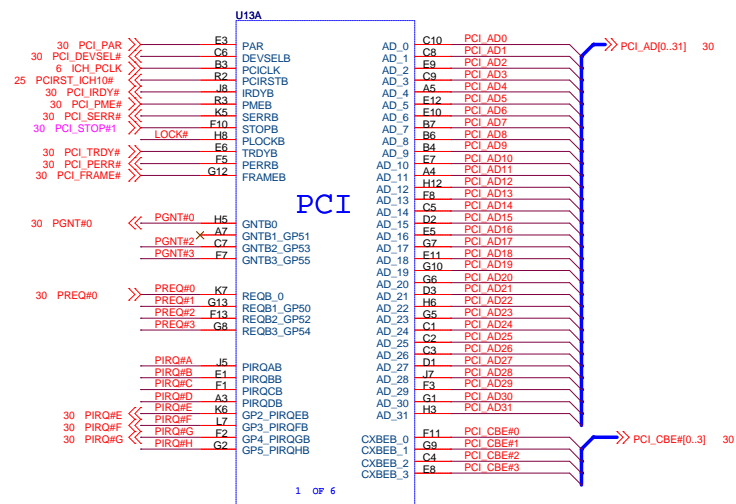
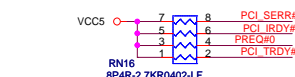
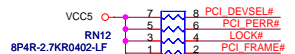
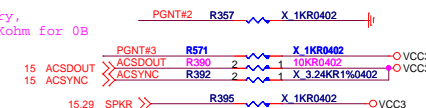
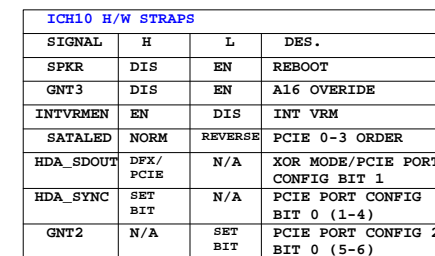


Diagram showing the connection for pins 1 to 8 of the P4R-2.7KR0402-LF component. The connections are as follows:

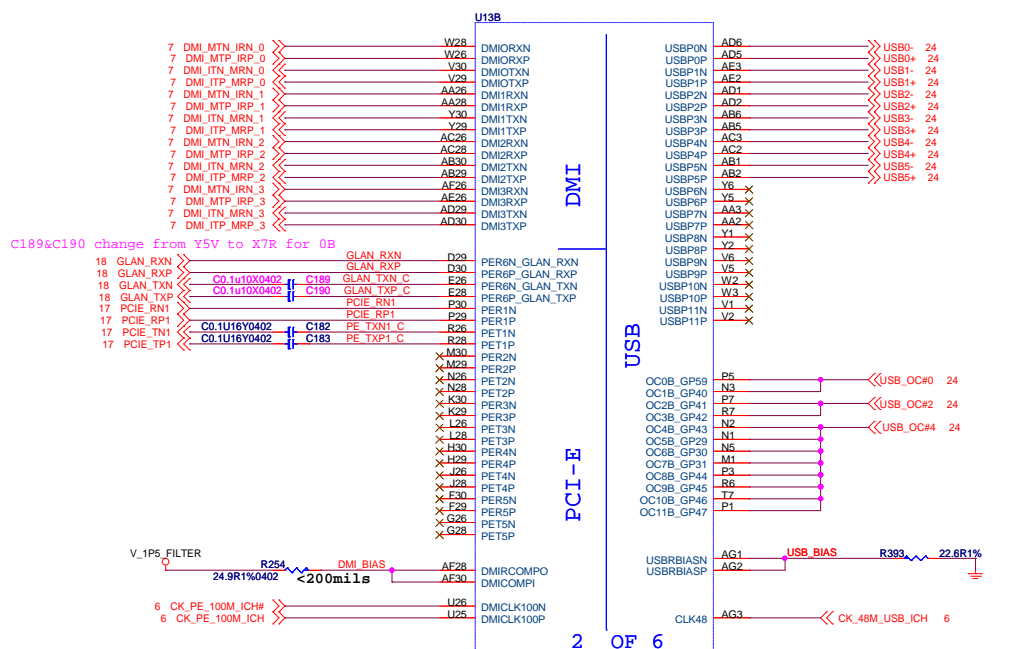
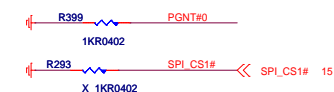
- Pin 1: VCC5
- Pin 2: PREQ#3
- Pin 3: RN11
- Pin 4: PCI\_STOP#1
- Pin 5: P4R-2.7KR0402-LF
- Pin 6: PREQ#1
- Pin 7: P4R-2.7KR0402-LF
- Pin 8: PREQ#1



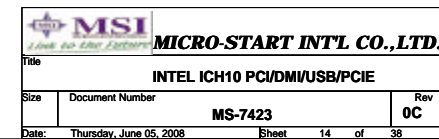
Support Danbury,  
R390 mount 10Kohm for 0B



BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	



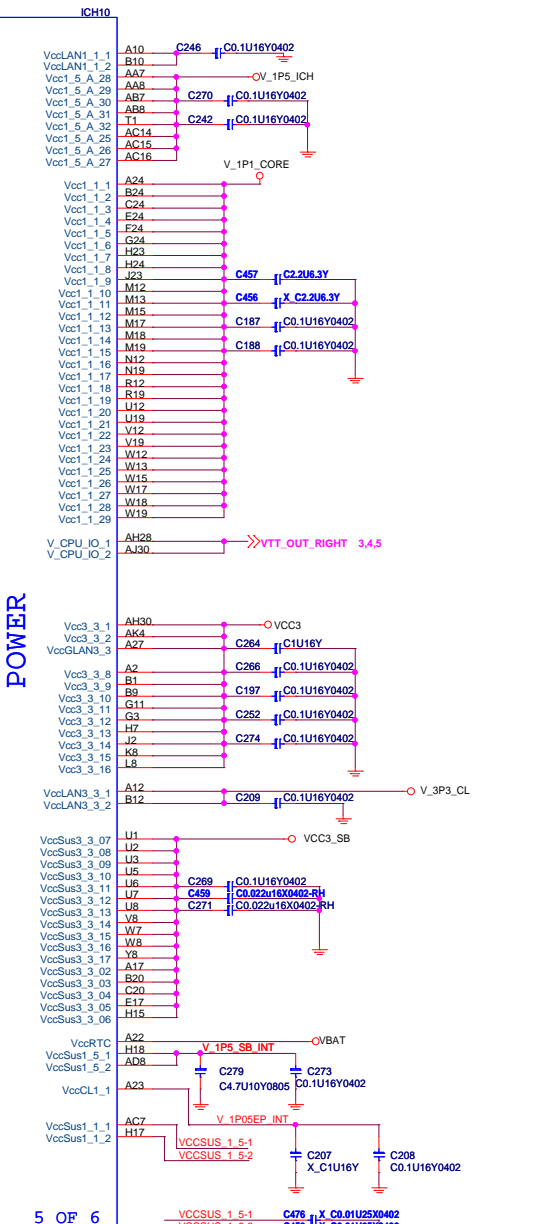
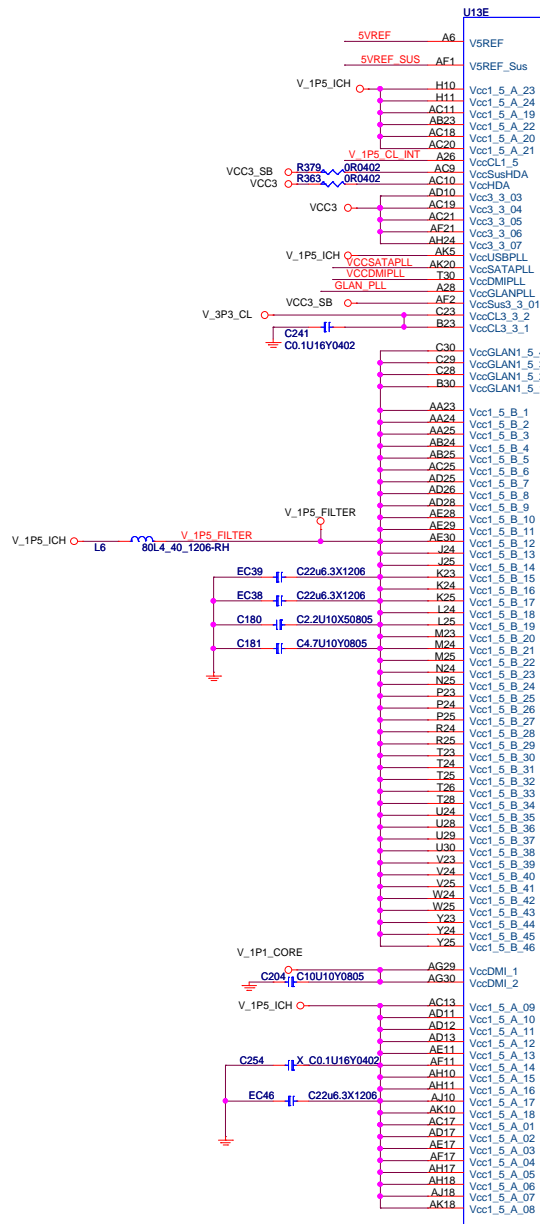
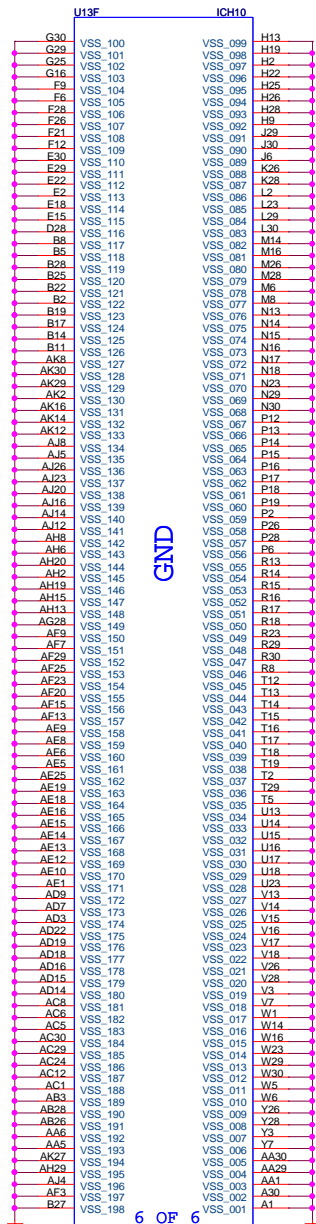
ICH10



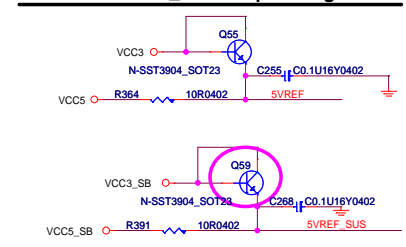




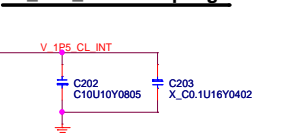




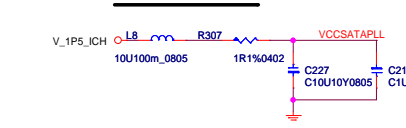
### 5VREF & 5VREF\_SUS Sequencing Circuit



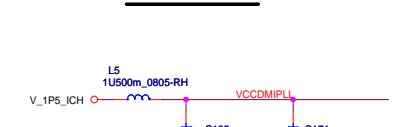
### V\_1P5\_CL decoupling



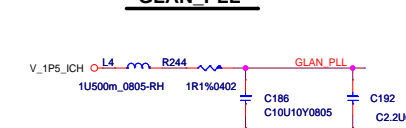
### VCCSATAPLL

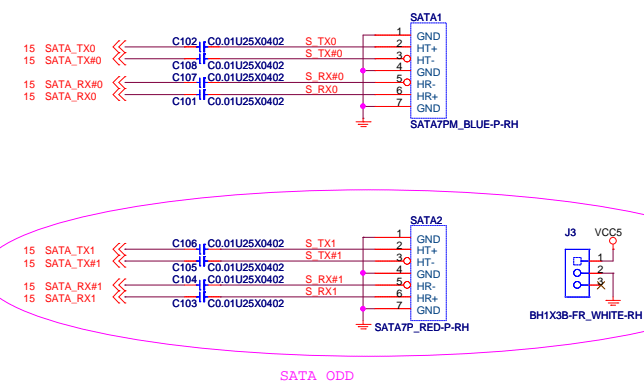


### VCCDMIPLL

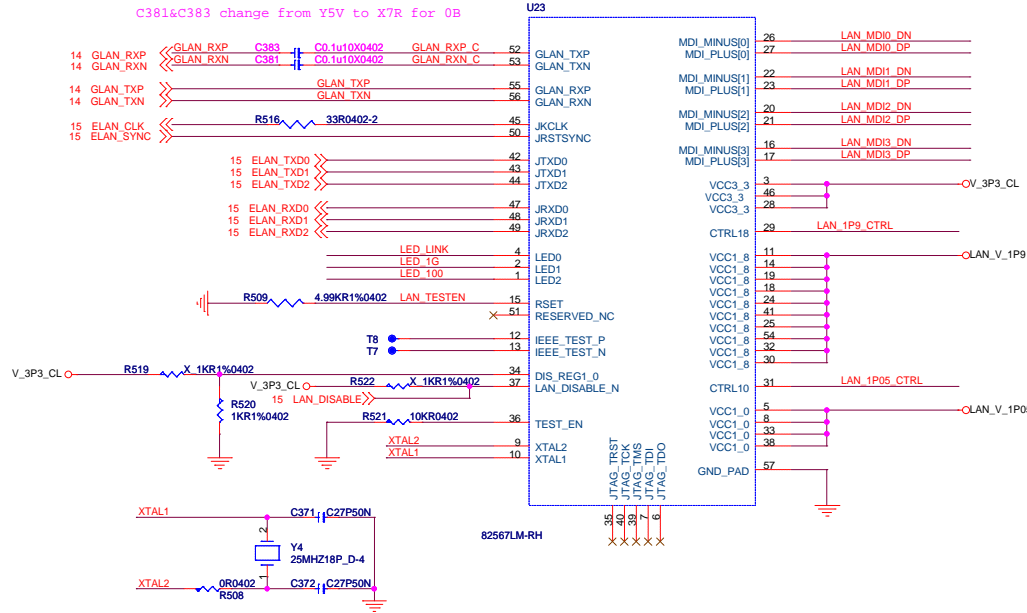


### GLAN\_PLL

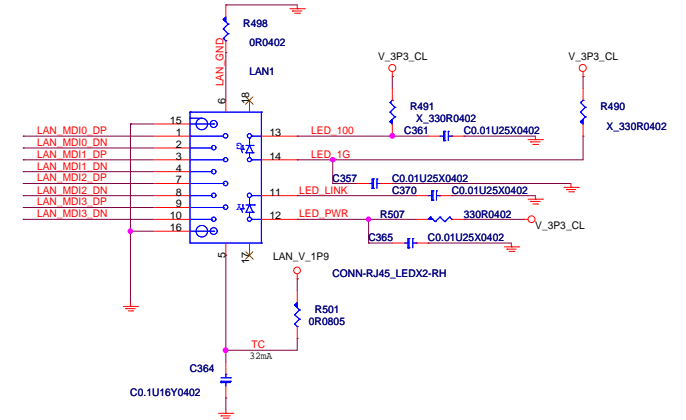


[illegible]

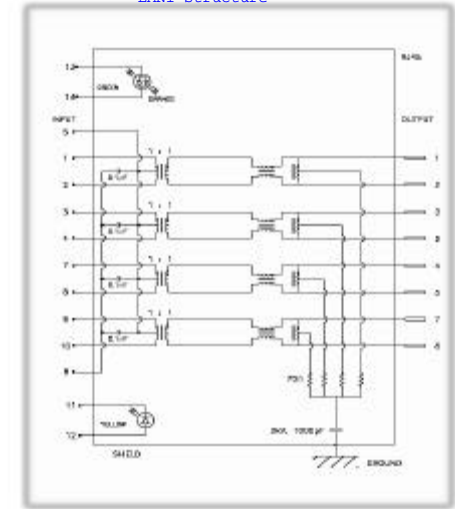
# INTEL 82567(Boanman)



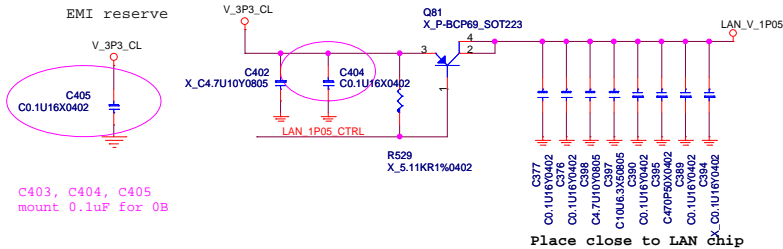
# LAN CONNECTOR



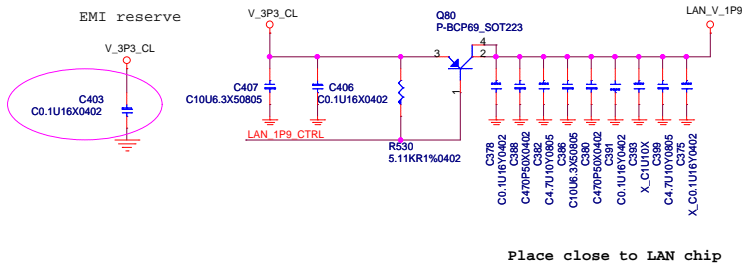
# LAN1 structure



# LAN 1P0 POWER (277.2mA)

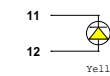
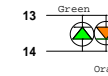


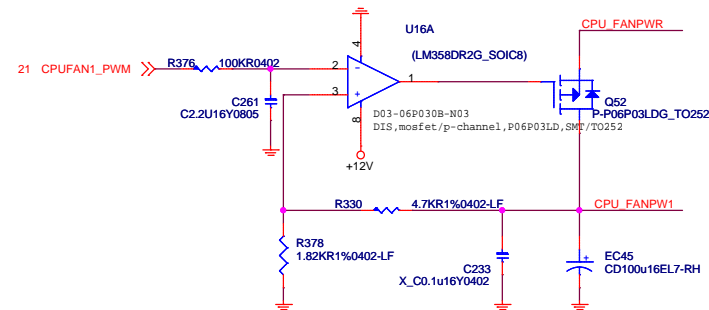
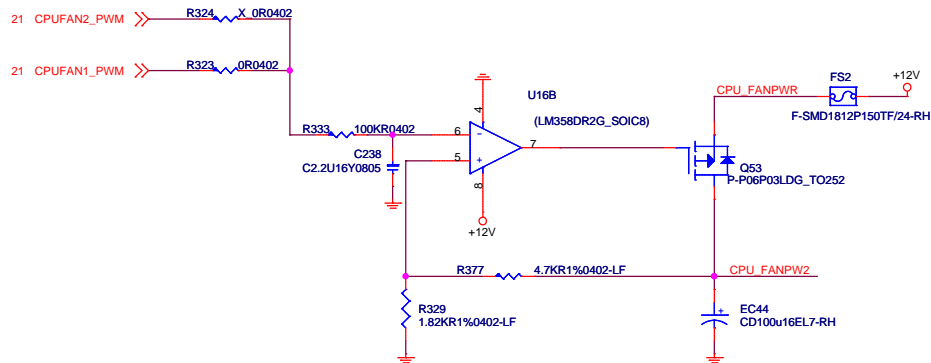
# LAN 1P8 POWER (418.2mA)



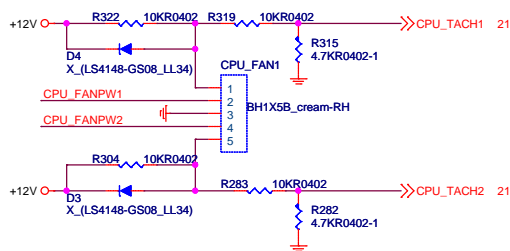
Speed LED Type  
100Mbps : Orange  
100Mbps : Green  
10Mbps : LED off

For Active/Link:  
Yellow

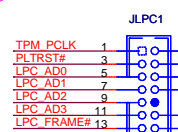




## CPU FAN



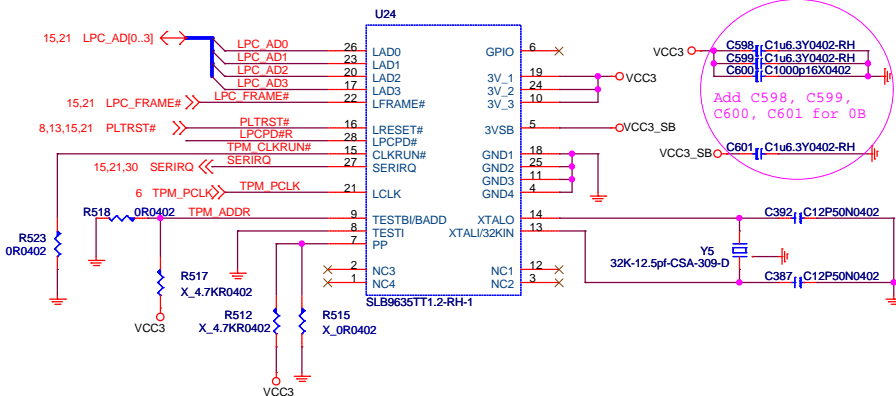
## LPC Debug Port



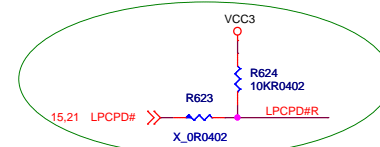
Add JLPC1 for 0B

## TPM 1.2

IO Address: 0x02E



added R624 and reversed R623 for 0C by Infineon's suggestion on 06/09

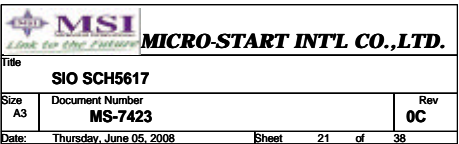


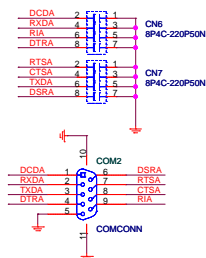
The four decoupling capacitors should be placed as short as possible to the respective 3V and 3VSB pins of the chip.

Add C598, C599, C600, C601 for 0B

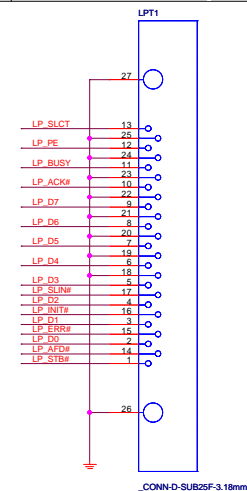
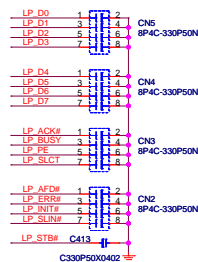
<b>MICRO-START INT'L CO.,LTD.</b>		
<b>TPM/FAN/LPC Debug Port</b>		
Size	Document Number	Rev
Custpm	<b>MS-7423</b>	<b>0C</b>
Date:	Monday, June 09, 2008	Sheet 19 of 38







21	LP_SLNW	LP_SLNW	1	2	2
21	LP_INTW	LP_INTW	3	4	RN24
21	LP_ERRW	LP_ERRW	5	6	6P4R-1KR-1
21	LP_AFDW	LP_AFDW	7	8	6P4R-1KR-1
		LP_D7	1	2	A
		LP_D6	3	4	A
		LP_D5	5	6	A
		LP_D4	7	8	RN26
					6P4R-1KR-1
21	LP_SLCT	LP_SLCT	1	2	A
21	LP_PE	LP_PE	3	4	A
21	LP_BUSY	LP_BUSY	5	6	RN28
21	LP_ACKW	LP_ACKW	7	8	6P4R-1KR-1
		LP_D3	1	2	A
		LP_D2	3	4	A
		LP_D1	5	6	A
		LP_D0	7	8	RN27
					6P4R-1KR-1
21	LP_STBW	LP_STBW	R542	1	RN402

[illegible]



# Video Connector

C198, C200, C201  
mount 10pF for  
0B by EMI  
suggestion

PLACE CLOSE TO MCH,  
WITHIN 250 MIL OF  
PIN

8 VGA\_RED <<

8 VGA\_GREEN <<

8 VGA\_BLUE <<

R268  
150R1%0402

R271  
150R1%0402

R266  
150R1%0402

C200  
C10p50N0402

C201  
C10p50N0402

C198  
C10p50N0402



PLACE CLOSE TO VGA CONNECTOR

L21  
0.15u300mA

L20  
0.15u300mA

L22  
0.15u300mA

R545  
150R1%0402

R544  
150R1%0402

R543  
150R1%0402

VCC5  
FS6  
F-MINISMDM150/24  
VGA 9.1

C426  
C0.1u16Y0402

JVGA1

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

VGA 15

VGA 14

VGA 13

VGA 12

VGA 11

VGA 10

VGA 9

VGA 8

VGA 7

VGA 6

VGA 5

VGA 4

VGA 3

VGA 2

VGA 1

VGA 0

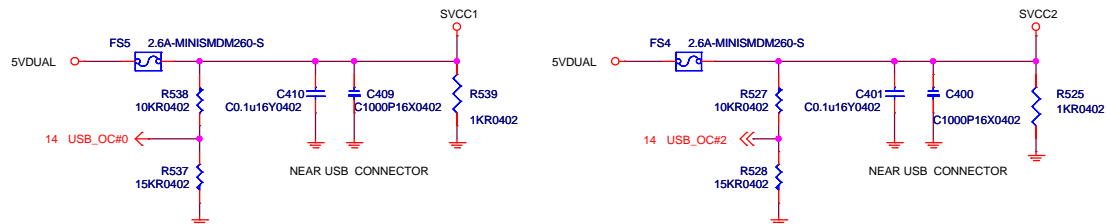
VGA 15

VGA 14

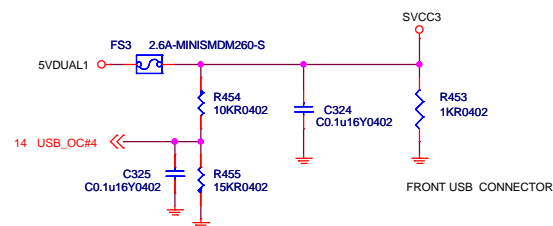
VGA 13

VGA 12

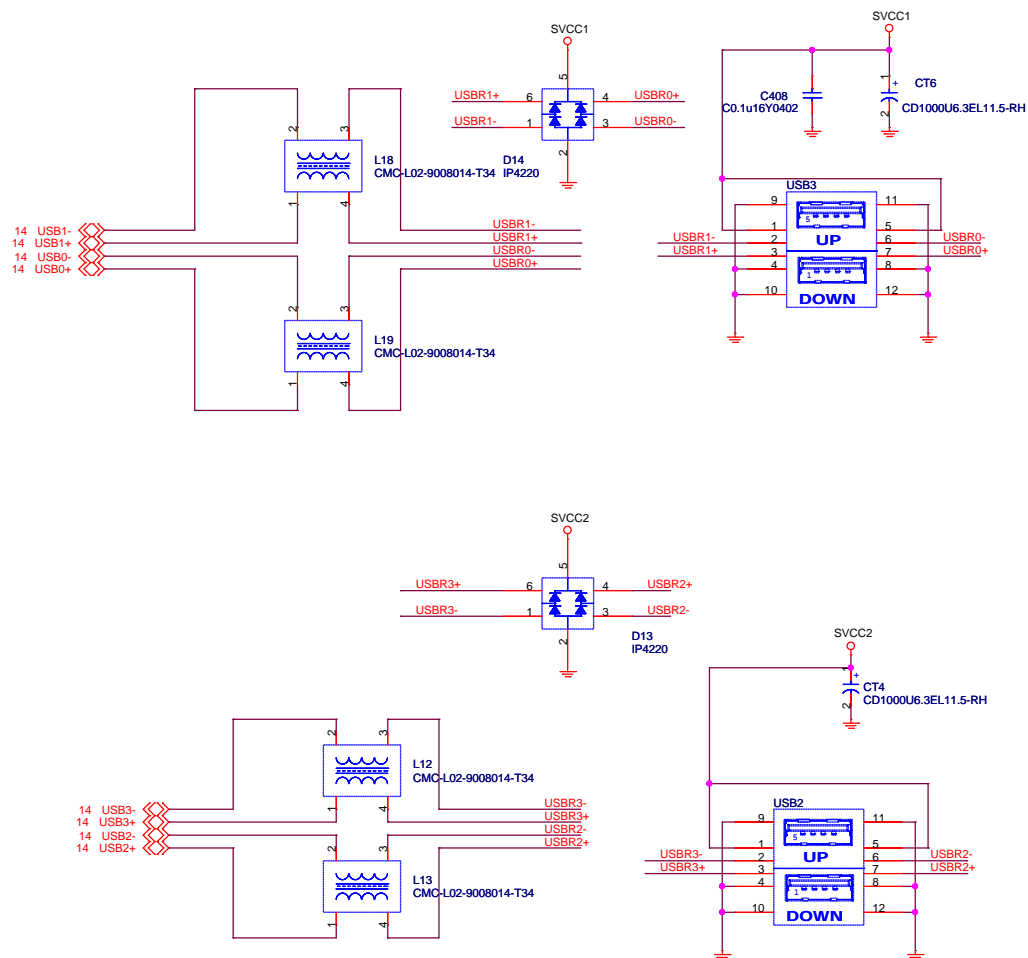
## POWER CIRCUIT FOR USB PORT 0,1,2,3



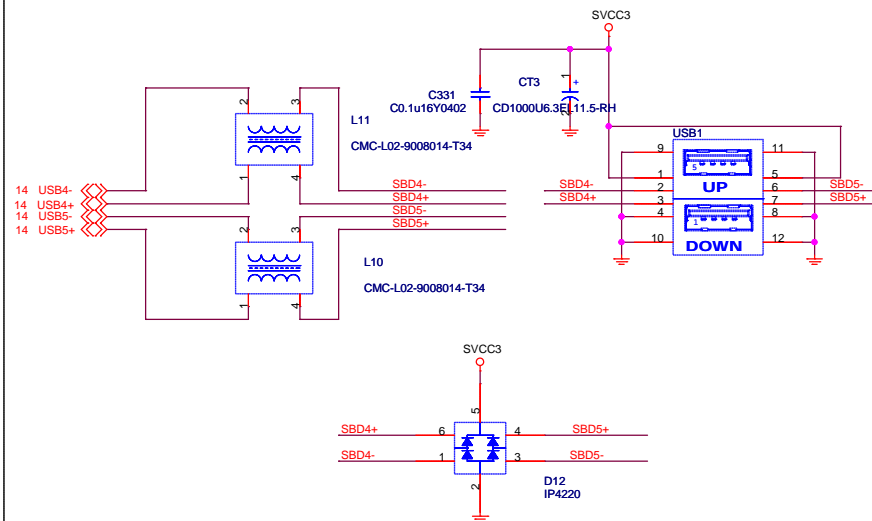
## POWER CIRCUIT FOR USB PORT 4,5



## REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3



## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

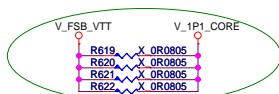
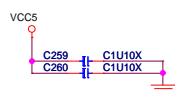


## VDIMM LINEAR OR PWM SELECT

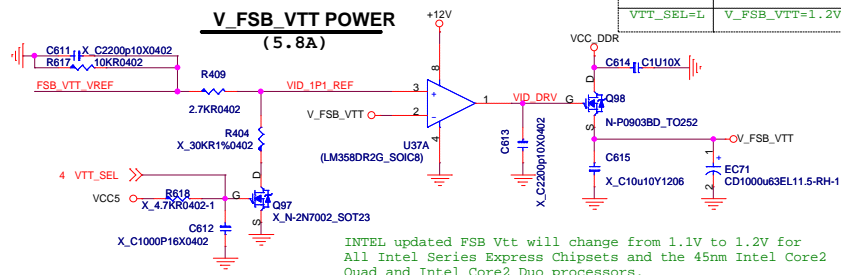
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

### 3VSB MODE SELECT

3VSB MODE	3VSDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

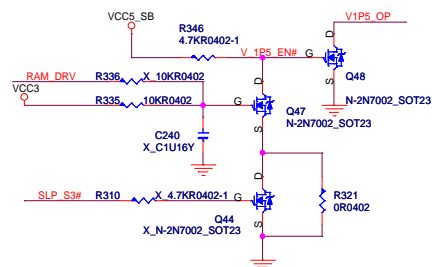


For 0C

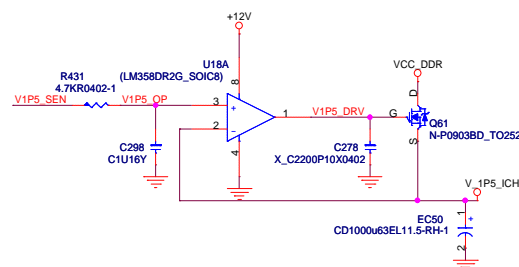
$$\frac{V_{FSB\_VTT} \text{ POWER}}{(5.8A)}$$


INTEL updated FSB Vtt will change from 1.1V to 1.2V for All Intel Series Express Chipsets and the 45nm Intel Core2 Quad and Intel Core2 Duo processors.

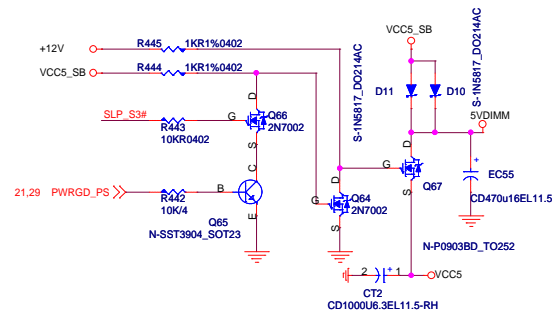
V1P5\_SEN S3 power sequency



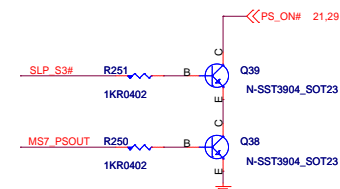
**ICH10 1.5V POWER**  
**(2.385A)**



## 5VDIMM



**PSON#**



**MICRO-START INTL CO.,LTD.**

Title			
ACPI CONTROLLER MS7			
Size	Document Number	Rev	
	MS-7423	0C	
Date:	Thursday, June 05, 2008	Sheet	25 of 38

EC62 change from 1000uF to 820uF for 0B

EC63 change from 1000uF to 820uF for 0B



# Intersil 6334

## 3Phases

R191 is changed from 1.91K ohm 1% to 1.5K ohm 1% by vendor's suggestion for 0B

R140 change 0603 type to 0805 type for 0B

R134, R124 for ISL6622CB

MOSFET Gate signal : 30 mils  
Phase signal : 30 mils  
Boot signal : 16 mils

MOSFET Gate signal : 30 mils  
Phase signal : 30 mils  
Boot signal : 16 mils

VRM solution change from DR.MOS to PowerPack for 0B

C126, C127, C129 are changed from 100pF to 68pF by vendor's suggestion for 0B

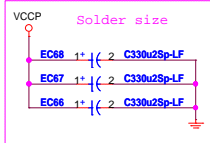
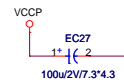
### ATX12V Power Connector

TDK NTCG104KF104FT

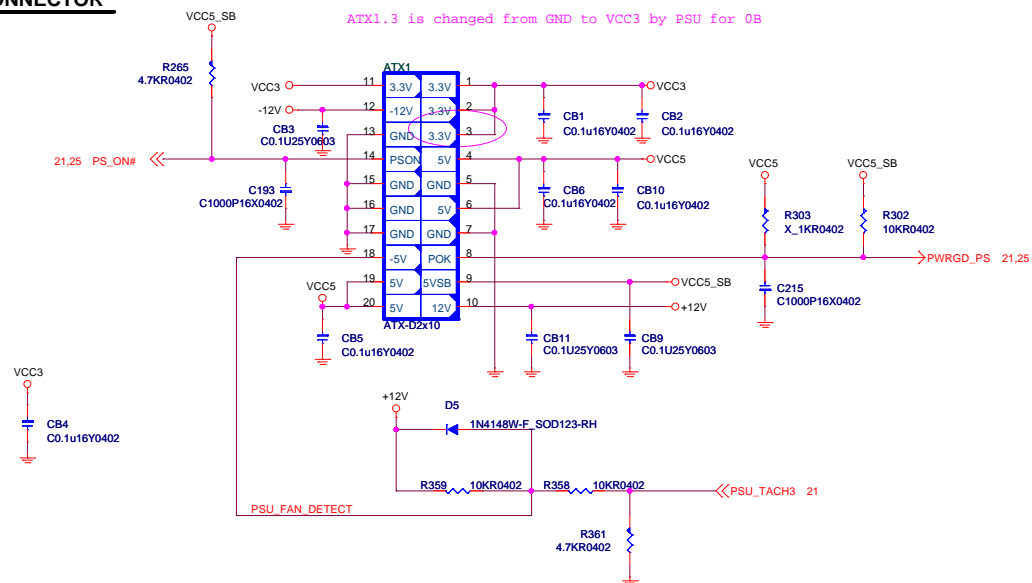
VR FAN TRIP: 1.69V ~ 80 degC  
VR HOT TRIP: 1.44V ~ 90 degC

### SP Capacitors

### SP Capacitors



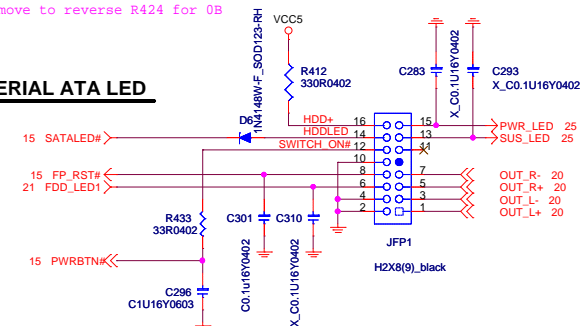
## ATX CONNECTOR



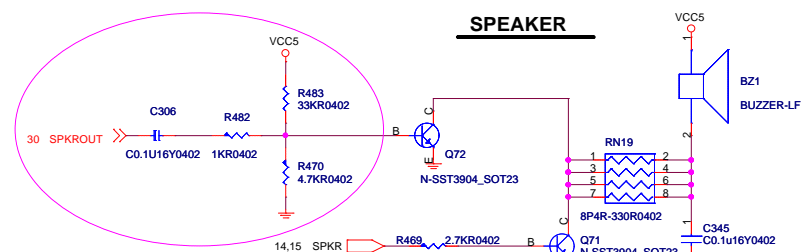
## Front Panel

remove to reverse R424 for 0B

## SERIAL ATA LED

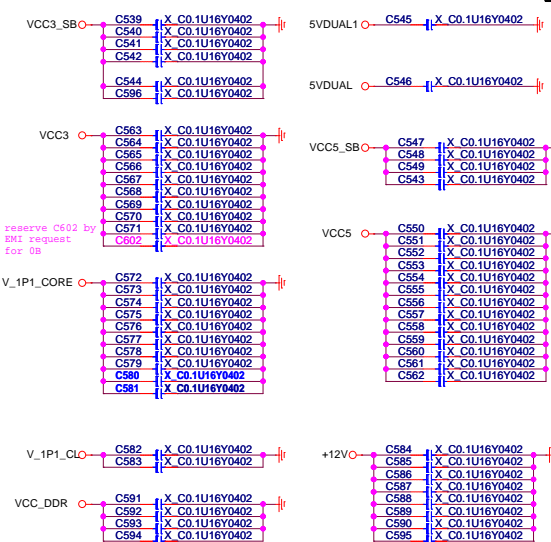


## SPEAKER



There would be improved by inserting some 32bits CardBus card

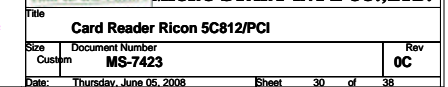
## EMI decoupling cap

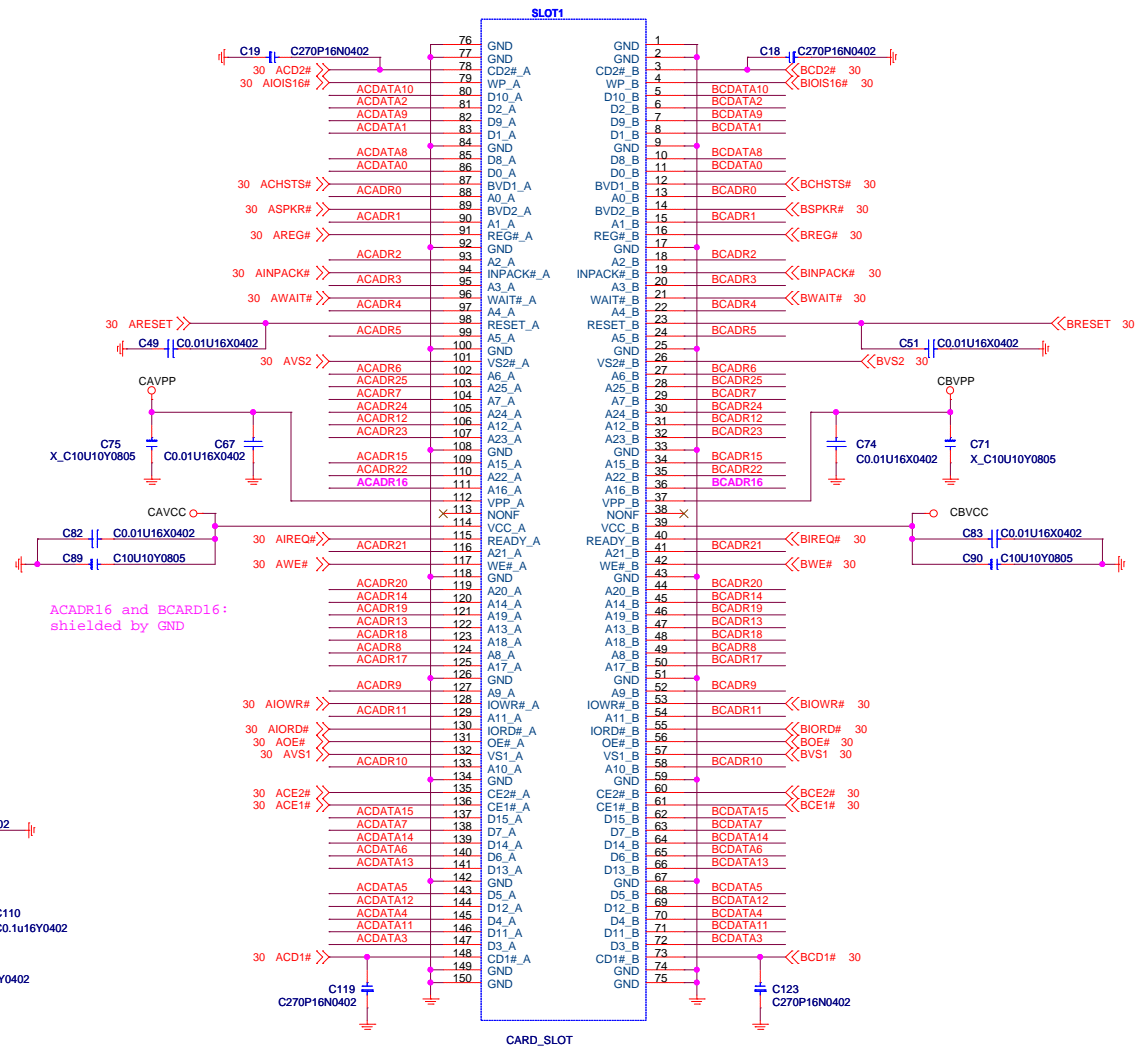
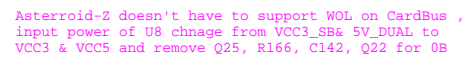


reserve C616, C617, C618 by EMI request for 0C

<b>MICRO-START INT'L CO.,LTD.</b>	
Title <b>ATX/Front Panel</b>	
Size Custom	Document Number <b>MS-7423</b>
Date: Friday, June 13, 2008	Rev <b>0C</b>
Sheet 29 of 38	









# ICH10

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPIO	BMBUSY# function, Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPIO	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPIO	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPIO	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPIO	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPIO	Pull-up to VCC3_SB with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPIO	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	LAN_DISABLE connect to LAN Boazman	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPIO	SIO_PME# connect to SIO, pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPIO	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# connect to CLK Gen and R5C812	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	NC	VCC3	UNMUXED	M2
GPIO 17	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO , Pull-up to VCC3 with 10K directly	VCC3	UNMUXED	K1
GPIO 19	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPIO	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull-up VCC3 with 10K(reserved)	VCC3	MUXED	J3
GPIO 24	I/O	GPO	NC	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# connect to CLK Gen	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE# pull-up to VCC3_SB with 1K ohm(reserved)	3.3V_SB		C11
GPIO 27	I/O	GPO	PANEL_DETECT pull up to VCC3 with 10Kohm	3.3V_SB		A11
GPIO 28	I/O	GPO	LCD_S1_ENA pull up to VCC3_SB with 10Kohm(reserved)	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	NC	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	Pull-up to VCC3 with 4.7K through JCI1 jumper.(Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	GPIO34 connect to HWSPND# directly	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	GP35 pull-up to VCC3_SB with 10Kohm(reserved)	VCC3		L1
GPIO 36	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPIO	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#4 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#4 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPIO	pull-up VCC3 with 10K	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping , pull-down 2.2K(reserved) to GND	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#(Unused)	VCC3	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC3 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#(Unused), pull-down 1K ohm(reserved) to GND	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Unused), pull-up 1K ohm(reserved) to VCC3	VCC3	MUXED	F7
GPIO 56	I/O	GPIO	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPIO	Pull-up to V_3P3_CL with 1K	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use) , SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18
GPIO 61	I/O		LPCPD# pull-up to VCC3_SB with 10Kohm(reserved)	3.3V_SB		R1
GPIO 62	I/O		NC	3.3V_SB		R5
GPIO 72	I/O		BATTLOW# pull-up to VCC3_SB with 10K ohm	3.3V_SB		C13

## SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP41	77	SIO_PME#	OUTPUT
GP25	30	SMBCLK	INPUT
GP26	29	SMBCLK_ISO	INPUT
GP35	28	SMBDATA	OUTPUT
GP42	27	SMBDATA_ISO	OUTPUT

## PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Ricoh R5C812	PIRQ#E PIRQ#F PIRQ#G	PREQ#0 PGNT#0	AD16	CK_PCMCIA

## PCI\_RST# DISTRIBUTION

SOURCE	PCIRST#	LOAD
ICH10	PCMCIA_RST#	Ricoh R5C812
	PCIRST_ICH10#	MS7
MS7	MINI_PCIE_RST#	MINI PCIE
	PLTRST#	TPM
	RSMRST#	ICH10
NB	H_CPUURST#	CPU

## DDR III DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	SCLK_A0/SCLK_A0#
		SCLK_A2/SCLK_A2#
DIMM 2	A4H	SCLK_B0/SCLK_B0#
		SCLK_B2/SCLK_B2#

## Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JCI1	(1-2)Normal	(2-3)ME Disable for FPROG
J4	(1-2)short: Normal	(1-2)Open: Clear PW

## SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH10, MINI PCI EXPRESS
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

 <b>MICRO-START INT'L CO.,LTD.</b>	
Title <b>GPIO MAP</b>	
Size	Document Number
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LGA775-CPU		
0.8375V - 1.6000V Core	-	84A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.33A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.3A

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Boazman GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6334		
VCCP VRD11.1	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

MS11+ SW-Power		
VCC_DDR	-	1.5V PWM 13.86A

MS11+ SW-Power		
V_1P1_CORE	-	1.1V PWM 23.27A

MS7 Controller		
V_1P1_CL	-	1.1V Linear 3A

V_1P5_ICH		
1.5V Linear	-	2.385A
VCC3_SB	-	3.3V Linear 3.96A
5VDUAL1	-	5V Switch 4.367A
5VDIMM	-	5V Switch 8.29A

DDRIII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	3.6A
1.5V VCC_DDR (S3)	-	TBDmA

LVDS		
2.5V	-	340mA
+3.3V	-	85mA

Mini PCI_E x1 slot		
+3.3Vaux	-	1100mA
1.5V	-	375mA

PCMCIA dual slot		
5V	-	1A
+3.3V	-	375mA

USB x 6		
+5V (S0,S1)	-	3A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

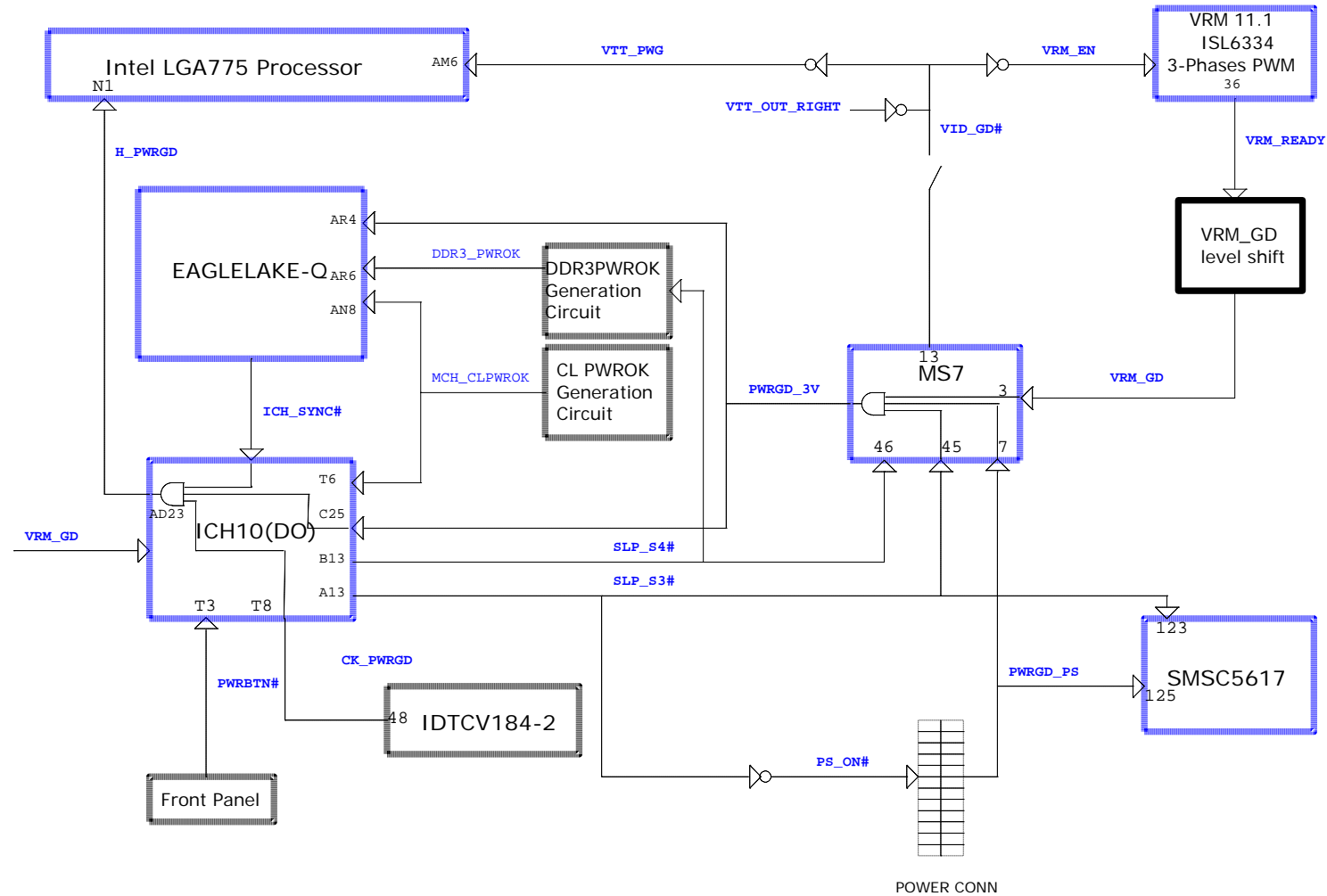
5VAudio		
+5VR	-	500mA

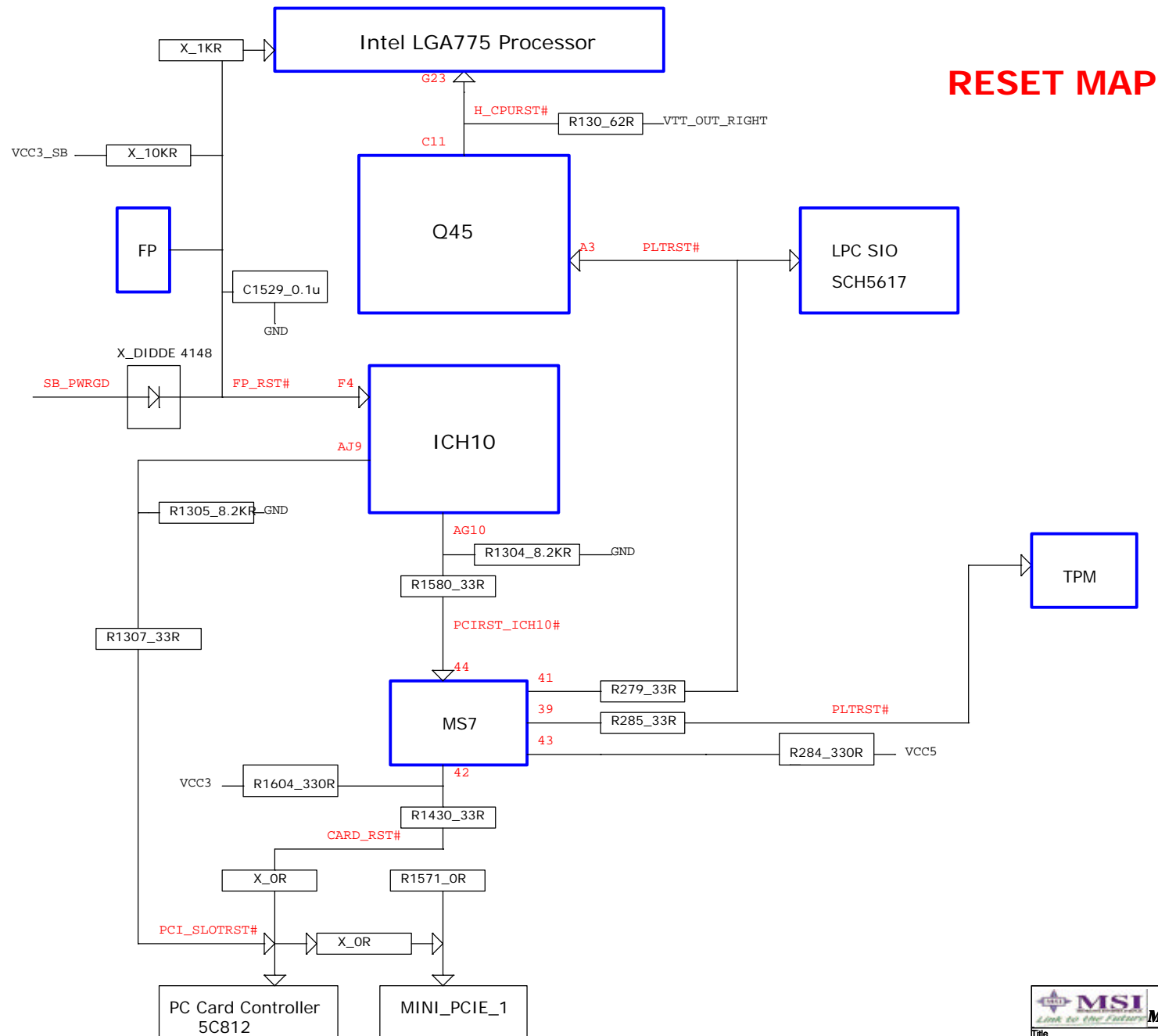
+12V		
ATX	-	2x2

ATX POWER			
+5V (10A)	+3.3V (12A)	+5VSB (10A)	+12V (12A)

PSU: DPS-200PB-168 A REV:S0F

# PWROK MAP







0A

(1) Remove the AC Coupling Capacitor(C306,C307) on Rx signal line. Because these Capacitor were mounted on Rxsignal line in MINI Card module board from NECP comment on page 17 on 2/20

0B

(1) Remove R152 and PM\_DPRSTR\_N(net) connect directly to U7.T2 on page 3

(2) R109, R111 not mount because they have unused on page 3

(3) U7.A23, U7.B23, U7.C23 change to test point on page 4

(4) Remove L1, R100, C87, C80, C92(they have unused), add Q92, R612, R613( add level shift between PROCHOT# and ICH10 (GPIO32) for NECP enconomy mode) on page 4

(5) Remove Q34, Q36, add Q91(unify the materials) on page 4

(6) C28, C29 are changed from 27pF to 47pF on page 6

(7) EC60 change from 1000uF to 820uF and EC58 mount 820uF on page 8

(8) R158 no mount, Q27 mount, remove R142, add Q34 (Intel PSI# design update)on page 8

(9) Remove Q54, Q56, add Q36, R385 mount(Intel suggestion), C262 change from 1uF to 12nF(Intel suggestion) on page 9

(10) C287 change from Y5V to X7R, C290 change from 0603 type/Y5V to 0402 type/X7R (follow Intel design)on page 9

(11) Remove R257 and L7 change from 10uH to 0ohm on page 10

(12) C44, C45 change from 27pF to 33pF on page 13

(13) Support Danbury, R390 mount 10Kohm on page 14

(14) Remove R409(it has unused), R332(immediately); R308 mount 33ohm(use ICH10 DRAMPWROK function pin); add GPIO\_32(net); R242, R245not mount (Intel suggestion) , R398 not mount(GPIO18 is already output function, don't need to pull-up); reserve C307(RC timing) on page 15

(15) C403, C404, C405 mount 0.1uF on page 18

(16) Added the four decoupling capacitors( C598, C599, C600, C601 ) should be placed as short as possible to the respective 3Vand 3VSB pins of the chip on page 19

(17) Add LPC debug port at JLPCL on page 19

(18) Solving the audio become to mute, rename to AC\_RST# (net) on page 20

(19) C528 is changed to T34(vendor) by buyer request on page 20

(20) Remove R500, R502(because they have unused), add D25(Due to Peci\_REQUEST have leakage, SMSC have workaround to add a diode to avoid )on page 21

(21) remove R492(immediately) and C367 change from 270pF to 220pF(the same as LE) on page 21

(22) Remove C224 on page 25

(23) EC62, EC63 change from 1000uF to 820uF ; EC61 mount 820uF; R437 & R439 not mount; Add C606, U36, R500, R502, C605, reverse C604; R177, R185 not mount; mount 1.1K $\Omega$  to R187; mount 12.4K $\Omega$  to R179, reverse C603; CHOKE6, CHOK5, COIL1, COIL2 change for transient and noise on page 26

(25) VRM solution change from DR.MOS to PowerPack(the same as LE), pls refer to page 28

(26) U13\_HS2 & U13\_HS3 are changed to the same AZ-S3 by mechanical request on 04/16

(27) R607, R608 are change from 6.8Kohm $\Omega$  to 18Kohm $\Omega$ , R572, R581 are change from 20Kohm $\Omega$  to 13Kohm $\Omega$  by customer request on page 20 on 04/17

(28) R140 change 0603 type to 0805 type(unify the materials) ; R137, R138, R139 are change from 4.7Kohm  $\Omega$  to 6.19.Kohm  $\Omega$  ; C126, C127, C129 are changed from 100pF to 68pF ; R191 is changed form 1.91K ohm  $\Omega$  to 1.5K ohm  $\Omega$  by vendor's suggestion on page 28

(29) U15 stepping change from A1 to A3 on page 7~11

(30) U13\_HS2 & U13\_HS3 change to the same Asteriod-S3 by mechanical request on 04/16

(31) Asteroid-Z doesn't have to support WOL on CardBus , all power of ICL chnage from VCC3\_SB to VCC3 , remove Q25, R166, C142, Q22 from NECP comment on page 30 & 31 on 04/18

(32) ATX1.3 is changed from GND to VCC3 by PSU , remove to reverse R424 for 0B on page 29

(33) C189&C190 change from Y5V to X7R on page 14

(34) C381&C383 change from Y5V to X7R on page 18

(35) U30, U32 are changed from SCHMITT-TRIGGER to BUFFER and are added R615, R614, R616 by customer request on page 20 on 4/22

(36) R387 and R388 not mount on page 9

(37) remove R404(reserved) on page 15

(38) remove to reserve R100 and R166 from CH7308B's datasheet rev2.1 on page 13

(39) C198, C200, C201 are mounted 1pF by EMI suggestion on page 23

(40) reserved decoupling cap to C602 by EMI request on page 29

(41) added HS5 & HS6 by mechanical request on page 32 on 04/25

(42) Add EC70 near CPU on page 26

(43) U13 stepping change to B0 on page 14 ~ 16


(44) EC2, EC6, EC10, EC13, EC18 are changed to a height of 11mm by mechanical & thermal request on page 13

(45) reserved C607,C608, C609, C610 by checklist request on page 21

(46) add FS7 by checklist request on page 13

(47) R3, Q1, Q2, R5, Q3 not mount because pin 27 of LCD\_1 is NC and BIOS no support S1 mode on page 13

A

		<b>MICRO-START INTL CO.,LTD.</b>	
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0B

(48) R601 and R606 are change from 47ohm 5% to 51ohm 1% by customer request on page 20 on 05/14

(49) R298, R350 not mount (pin 27 of LCD\_1 is NC pin) and R350 not mount(BIOS no support S1 mode) on page 15

(50) R456, C326, R457, R451, R452 not mount on page 27

0C

- (1) Power name change from V\_PLI\_CORE to V\_FSB\_VTT on page 3, 4, 7, 10, 11
- (2) C138 mount 220pF on page 4
- (3) R279 change from 1Kohm to 1.02Kohm on page 8
- (4) D25 change from 4148 to 5817 on page 21
- (5) Intel updated FSB Vtt will change from 1.1V to 1.2V for all Intel Series Express Chipsets and the 45nm Intel Core2 Quad and Intel Core2 Duo processors on page 25
- (6) Due to V\_FSB\_VTT become to 1.2V ,VTT\_DDR POWER increase to 19.66 A, so add a low size MOS(Q99) for DDR POWER on page 26
- (7) Added R624 and reversed R623 for 0C by Infineon' s suggestion on page 19 on 06/09
- (8) Remove R365 because of unuse on page 10
- (9) Reserve C616, C617, C618 by EMI request on page 29